DC OFFSETS IN COMMUNICATION SYSTEMS

BACKGROUND OF THE INVENTION

Related Applications

[0001] This application claims priority to U.S. Provisional Application Serial No. 60/390,585, filed on June 20, 2002.

Field of the Invention

[0002] The present application relates, in general, to wireless data communications systems in the presence of noise.

DESCRIPTION OF THE RELATED ART

[0003] Data is information that is in a form suitable to manipulation and/or processing in a formalized manner, such as by one or more machines. Wireless data communications systems are systems that transmit and/or receive data through at least one wireless data communications link (e.g., through the air or through a vacuum).

[0004] With reference to the figures, and with reference data Figure 1, shown is a high-level block diagram of a wireless data communications system 150. Depicted is a human user 152 speaking into a microphone 154. Illustrated is that the microphone 154 converts the continuous sound energy speech of the human user 152 into continuous electrical signals. Shown is that a sampler 156 converts the continuous electrical signals into discrete electrical signals. Depicted is that a quantizer 158 quantizes each discrete electrical signal into a unique specific pulse amplitude modulation voltage. Illustrated is that encoder 160 encodes each quantized discrete electrical signal into a string of bits. Shown is that symbol encoder 162 encodes one or more bits in the string of bits into a symbol as dictated by a symbol scheme, where each symbol in the scheme can be viewed as a sum of two orthogonal vectors (e.g., I and Q vectors).

[0005] Depicted is that the symbol encoder 162 outputs the appropriate values of the I and Q vectors such that their vector sum results in the appropriate value under the defined signal scheme. Illustrated is that the value of the I vector is used to modulate a

first sine wave (defined as the "in-phase" (I) sine wave since it is associated with the I vector), and that the value of the Q vector is used to modulate a second sine wave (defined as the "quadrature-phase" (Q) since it is 90 degrees out of phase with the first (I) sine wave). Shown is that the I and Q modulated sine waves are added in summation block 164 to produce a composite signal which is then received by modulator 166 to modulate a carrier sine wave. Depicted is that the modulated carrier sine wave is then transmitted through antenna 168 and into the wireless data communications link 170.

[0006] Depicted is that demodulator 172 receives the modulated carrier sine, wave via antenna 170, which is then fed to Automatic Gain Control unit (AGC) 173. Those skilled in the art will appreciate that AGC 173 provides for automatic adjustment of a gain, as a function of the strength of the modulated carrier received via antenna 170, in order to maintain a relatively constant output signal level. Illustrated is that demodulator 172 demodulates the automatic gain controlled version of the received signal down to a composite signal which is received by both in-phase (I) sine wave demodulator 174 and a quadrature-phase (Q) demodulator 176, which respectively output the values of the I vector and Q vector. Thereafter, shown is that symbol decoder 178 uses the values of the I vector and Q vector to produce one or more symbol bits, which are then passed to D/A converter 180. Depicted is that D/A converter outputs a continuous electrical signal which is converted into sound energy by speaker 182.

BRIEF DESCRIPTION OF THE FIGURES

[0007] Figure 1 illustrates a high-level block diagram of a wireless data communication system.

[0008] Figure 2 illustrates a portion of the wireless data communication system of Figure 1.

[0009] Figure 2 illustrates a portion of the wireless data communications system of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

[0010] Referring to the Figure 2, depicted is a portion of the wireless data communications system of Figure 1. Illustrated is that in an "ideal," or theoretical, system, both the I and Q components are always detected correctly, and thus the symbol decoder 178 always decodes the symbol correctly. Shown is that in an actual, physical system, as opposed to an ideal or theoretical system, system irregularities give rise to direct current (DC) offset voltages. Depicted is that, insofar as symbol decoder 178 relies upon both the sign and magnitude of the detected voltages of the respective I and Q components in order to correctly decode a received symbol, the presence of DC offset voltages, which can give rise to an offset of either or both the I and Q components, can result in symbol decoder 178 incorrectly decoding a received symbol. Although those having ordinary skill in the art will appreciate that symbol decoder 178 is representative of a quadrature phase shifted keyed (QPSK) decoder, those skilled in the art will also appreciate that symbol decoder 178 is exemplary of decoders which decode in the presence of noise.

[0011] In addition to the foregoing, those having ordinary skill in the art will appreciate that due to the effects of the AGC 173, the DC offsets will tend to vary over time, which tends to make it difficult to compensate for the foregoing-described deleterious effects of DC offsets. Fortunately, the inventor has devised methods and systems which will substantially allow compensation of DC offsets which may be present, irrespective of whether AGC 173 is causing such DC offsets to change over time. One implementation of such methods and systems is shown and described in relation to Figure 3.

[0012] With reference now to Figure 3, shown is a portion of the wireless data communications system of Figure 2, modified such that a time-averaged value of the DC offsets of either or both the I and Q components are removed from the I and Q components before symbol decoding. Depicted is that the output of in-phase (I) sine wave demodulator 174 is fed into a very low pass filter (e.g., a DC filter) 300 and time-averaged DC component subtracter unit 302. Illustrated is that the output of the very low pass filter 300 is fed into an I-component DC voltage estimator circuit 304. Shown is that the output of the I-component DC voltage estimator circuit 304 is fed into the I-component DC

voltage averaging unit 303, which calculates the average of its DC input voltage over some defined period of time. Shown is that the output of the I-component DC voltage averaging unit 303 is fed into a time-averaged DC component subtracter unit 302. Depicted is that the time-averaged DC component subtracter unit 302 removes the time-averaged DC component from the I-component output of the in-phase (I) sine wave demodulator 174. Illustrated is that the output of the time-averaged DC component subtracter unit 302 is fed into the symbol decoder 178.

[0013] Depicted is that the output of quadrature-phase (Q) demodulator 176 is fed into a very low pass filter (e.g., a DC filter) 306 and a time-averaged DC component subtracter unit 308. Illustrated is that the output of the very low pass filter 306 is fed into a Q-component DC voltage estimator circuit 310. Shown is that the output of the Q-component DC voltage estimator circuit 306 is fed into the Q-component DC voltage averaging unit 305, which calculates the average of its DC input voltage over some defined period of time. Shown is that the output of the Q-component DC voltage averaging unit 305 is fed into the time-averaged DC component subtracter unit 308. Depicted is that the time-averaged DC component subtracter unit 308 removes the average DC component from the Q-component output of the quadrature-phase (Q) demodulator 176. Illustrated is that the output of the time-averaged DC component subtracter unit 308 is fed into the symbol decoder 178.

[0014] Those having ordinary skill in the art will recognize that the state of the art has progressed to the point where there is little distinction left between hardware and software implementations of aspects of systems; the use of hardware or software is generally (but not always, in that in certain contexts the choice between hardware and software can become significant) a design choice representing cost vs. efficiency tradeoffs. Those having ordinary skill in the art will appreciate that there are various vehicles by which aspects of processes and/or systems described herein can be effected (e.g., hardware, software, and/or firmware), and that the preferred vehicle will vary with the context in which the processes and/or systems are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a hardware and/or firmware vehicle; alternatively, if flexibility is paramount, the implementer may opt for a solely software implementation; or, yet again alternatively, the

implementer may opt for some combination of hardware, software, and/or firmware. Hence, there are several possible vehicles by which aspects of the processes described herein may be effected, none of which is inherently superior to the other in that any vehicle to be utilized is a choice dependent upon the context in which the vehicle will be deployed and the specific concerns (e.g., speed, flexibility, or predictability) of the implementer, any of which may vary.

[0015] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and examples. Insofar as such block diagrams, flowcharts, and examples contain one or more functions and/or operations, it will be understood as notorious by those within the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof. In one embodiment, the present invention may be implemented via Application Specific Integrated Circuits (ASICs). However, those skilled in the art will recognize that the embodiments disclosed herein, in whole or in part, can be equivalently implemented in standard Integrated Circuits, as one or more computer programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more controllers (e.g., microcontrollers) as one or more programs running on one or more processors (e.g., microprocessors), as firmware, or as virtually any combination thereof, and that designing the circuitry and/or writing the code for the software and or firmware would be well within the skill of one of ordinary skill in the art in light of this disclosure. In addition, those skilled in the art will appreciate that the mechanisms of the present invention are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the present invention applies equally regardless of the particular type of signal bearing media used to actually carry out the distribution. Examples of signal bearing media include, but are not limited to, the following: recordable type media such as floppy disks, hard disk drives, CD ROMs, digital tape, and computer memory; and transmission type media such as digital and analogue communication links using TDM or IP based communication links (e.g., packet links).

[0016] The foregoing described embodiments depict different components contained within, or connected with, different other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected", or "operably coupled", to each other to achieve the desired functionality.

[0017] While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that, based upon the teachings herein, changes and modifications may be made without departing from this invention and its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as are within the true spirit and scope of this invention. Furthermore, it is to be understood that the invention is solely defined by the appended claims. It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," etc.). It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to inventions containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite

articles such as "a" or "an" (e.g., "a" and/or "an" should typically be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation *is* explicitly recited, those skilled in the art will recognize that such recitation should typically be interpreted to mean *at least* the recited number (e.g., the bare recitation of "two recitations," without other modifiers, typically means *at least* two recitations, or *two or more* recitations).

[0018] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.